REMARKS

Claims 1-9 are pending in this application. By this Amendment, claims 1-4 are amended. No new matter is added.

I. Allowable Subject Matter

Applicants appreciate the Office Action's indication that claim 3 is allowed and that claims 2, 4 and 5 contain allowable subject matter.

II. Rejections under 35 U.S.C. §102

The Office Action rejects claims 1 and 6-9 under 35 U.S.C. § 102(e) over U.S. Patent No. 6,754,279 (Zhou). This rejection is respectfully traversed.

Claim 1 recites, in part, "an output control signal generating circuit that generates an output control signal that controls whether each component of the input image data is output or not based on a decimation pattern that is determined depending on a format of the input image data and a reduction ratio, the reduced image data generating circuit including a switching circuit that controls a presence of output for each component of the input image data being input in series based on the output control signal."

First, Zhou fails to teach or suggest the claimed output control signal generating circuit. Instead, Zhou teaches a digital still camera architecture in which captured images are stored as JPEG bit streams (col. 9, lines 49-51). In playback mode, the JPEG data is decoded at the resolution of a CCD sensor (col. 9, lines 59-60) and for display purposes this decoded data has to be down-sampled to NTSC resolution before it can be fed into the NTSC encoder (col. 2, lines 62-65). In Zhou, the down-sampling scheme, which includes anti-aliasing filtering and decimation, is included as part of the JPEG decompression module (col. 10, lines 2-4). The third stage of JPEG decompression is an inverse discrete cosine transform that is performed on a block of 8 x 8 pixels (col. 10, lines 4-8). In JPEG decompression, the inverse discrete cosine transform employs an 8-to-4 decimation (col. 10, lines 18-19). Thus,

the alleged decimation pattern of the input component is not determined depending on a format of input image data and reduction ratio. Rather, since the images are stored as JPEGs, Zhou always employs 8-to-4 decimation.

Second, Zhou fails to disclose the claimed reduced image data generating circuit including a switching circuit. Instead, Zhou's CCD module 150 (allegedly corresponding to the reduced image generating circuit) comprises a CCD imager, driver electronics and a timing generator for the necessary signals to clock the CCD, correlated double sampling and automatic gain control electronics (col. 2, lines 34-36). Thus, the CCD module 150 does not include switching circuit that controls a presence of output for each component of image data input in series based on the output control signal. Rather, the CCD module 150 in Zhou interfaces directly to the DSC engine 100 using the built-in CCD/CMOS controller 102 to output a real-time data stream as pictures are taken (col. 3, lines 1-6 and 16-18).

For at least these reasons, Zhou does not teach or suggest all the features of claim 1. Therefore, withdrawal of the rejection of claim 1 and claims 6-9 depending therefrom is respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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